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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,417	04/15/2004	Jang Hwan Cho	YHK-0111	6471

34610 7590 01/22/2008
KED & ASSOCIATES, LLP
P.O. Box 221200
Chantilly, VA 20153-1200

EXAMINER	
SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,417	CHO ET AL.	
	Examiner	Art Unit	
	Grant D. Sitta	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/11/2005,11/3/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: filing date for co-pending (OP3095) and (OP3096) needs to be completed (bottom of page 14 and top of page 15).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Rilly et al (5,808,420) hereinafter Rilly.

3. In regards to claim 1, Rilly teaches a plasma display (abstract, "plasma display"), comprising: a panel (abstract, "screen or panel"); at least one voltage source (fig. 3 (V1 and V2)) for supplying a sustain voltage to the panel; an inductor (fig. 3 (L)) for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel; and first (fig. 3 (T1)) and second (fig.

3 (T2)) switches arranged, in parallel (fig. 3 T1, T2, and L parallel relationship), between the inductor and the panel (col. 3, lines 1-48).

4. In regards to claim 5, Rilly teaches an energy recovering (abstract, "recovery of the energy") method for a plasma display (abstract, "plasma display"), comprising: forming a first electrically conductive path between a first voltage source (fig. V1 (col. 3, lines 1-48) and the plasma display using a first switch (fig. 3 one of switches T6s); forming a second electrically conductive path between a second voltage source (fig. 3 V2 (col. 3, lines 1-48).) and the plasma display using a second switch (fig. 3 one of switches T4)); forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 3 (T1)); and forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected (fig. 3 T2), in parallel (fig. 3 T1, T2, and L parallel relationship), to the third switch (col. 3, lines 1-48).

5. In regards to claim 2, Rilly teaches wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity (fig. 3 (V1)); and a second voltage source (fig. 3 (V2)) for charging the panel to a second polarity different from the first polarity. ("It can be seen that the voltage values V2 and V1 are of different magnitude, for matching to the plasma screen, for example V2=120 volts and V1=-150 volts." Col. 3, lines 40-45).

6. In regards to claim 3, Rilly teaches further comprising: a third switch (fig. 3 (T6s)) for forming a conductive path between the first voltage source (fig. 3 V1) and the panel; and a fourth switch (fig. 3 T4s) for forming a conductive path between the second voltage source (fig. 3 V2) and the panel.

7. In regards to claim 4, Rilly teaches: a first diode connected between the first switch and the panel (fig. 3 one of D6s); and a second diode connected between the second switch and the panel (fig. 3 one of D4s).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 6-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rilly.

11. In regards to claim 7, Rilly discloses the limitations of a display having a plurality of electrodes and having a corresponding display (abstract, "plasma display") capacitance (abstract "to the general capacitance of the screen or panel ") between first fig. 3 (N)) and second nodes (fig. 3 ground); an inductor (fig. 3 (L)) coupled to the second node and a third node; a first switch coupled between the first and third nodes (fig. 3 (T1)); and a second switch coupled between the first and third nodes (fig. 3 (T2)), the first and second switches being formed in parallel (fig. 3 (T1 and T2 are in parallel from ground), wherein a first current path is formed via the panel capacitance (fig. 3 Cp), the second node, the inductor (fig. 3 (L)), the third node, the first switch and the first node, and a second current path is formed via the panel capacitance (fig. 8 and 10 (col. 3-4, lines 47-40) the first node, the second switch (fig. 3 (T2)), the third node, the inductor (fig. 3 (L)) and the second node (col. 2-3, lines 25-45),

Rilly differs from the claimed invention in that the switches (switches T4(+ and -) and T6(+ and -) are located between the inductor and ground instead of between the inductor and capacitor.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Rilly to include the use of a switch between inductor and capacitor since the circuit won't be conducting unless the switch is closed.

2. In regards to claim 19, Rilly teaches display panels (abstract, "plasma display") having panel electrodes and corresponding panel capacitance between first and second nodes (fig. 3 (cp)), an inductor (fig. 3 (L)) coupled to the second node and a third node, a first switch (fig. 3 (T1)) coupled between the first and third nodes and a second switch (fig. 3 (T2)) coupled between the first and third nodes, the first and second switches being formed in parallel (fig. 3 T1 and T2 are in parallel from ground),

(a) discharging the panel capacitance (fig. 3 (cp)) through said inductor (fig. 3 (L)) initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a first current path (fig. 4, 10 and 12) formed via the panel capacitance (fig. 8 C panel), the second node, the inductor (fig. 3 (L)), the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current (col. 3-4, lines 58-40) reaches zero or before zero via the first current path (figs. 8 and 10 col. 3-4, lines 58-40); and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum (col. 1, lines 25-67) through a second current path formed via the panel capacitance

(col. 2, lines 25-67), the first node, the second switch (fig. 3 T2), the third node, the inductor (fig. 3 (L)) and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current path (fig. 8-10 IL, Ip and Vp).

3. In regards to claim 25, Rilly teaches a plasma display panel driver circuit comprising: a panel inter-electrode capacitor (fig. 3 Cp) provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel (abstract "plasma"); a charging/discharging circuit (fig. 3 (L and circuit components)) connected in series with said panel inter-electrode capacitor (fig. 3 (Cp)) and between first and second nodes, a clamping circuit (fig. 5 D4 and D6(+ and -)) having first (T1) and second (T2) switches for clamping a terminal voltage across the panel inter-electrode capacitor (fig. 3 Cp) to a first power source voltage level (V1) and to a second power source voltage level (V2), said first switch being connected in series between the first node and the first power source voltage level (col. 3 lines 10-60), said second switch being connected in series between said first node and the second power source voltage level, said inter-electrode capacitor (fig. 3 (Cp)) being connected in series to the first and second nodes and said charging/discharging circuit (fig. 3 (L and circuit components)) and said clamping circuit being coupled in parallel between the first and second nodes (fig. 5 D5(+ and -)), wherein said charging/discharging circuit (fig. 3 (L

and circuit components)) comprises a pair of switches coupled in parallel to each other between the first anode and a third node and an inductive coil coupled in series between the second and third nodes (fig. 3 L, Cp, and D5(+ and -) and col. 3, lines 10-60).

4. In regards to claim 6, Rilly teaches shutting off a backward current from the plasma display using a first diode connected between the third switch and the plasma display; and shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display (fig. 4 T6 (+ and -) and T4 (+ and -).

5. In regards to claim 8, Rilly teaches wherein the direction of the first and second current paths are opposite directions (fig 10 (IL) positive and negative charges).

6. In regards to claim 9, Rilly teaches wherein the first current path charges the display capacitance from a first potential to a second potential and the second current path discharges the display capacitance from the second potential to the first potential (fig 10 (IL) positive and negative charges and col. 2, lines 25-67).

7. In regards to claim 10, Rilly teaches wherein the display capacitance is charge or discharged based on an LC resonance frequency (col. 3, lines 28-31 fig. 3 L and C).

8. In regards to claim 11, Rilly teaches wherein the display capacitance is charged or discharged based on a non-LC resonance frequency (col. 3, lines 20-67 fig. 3 T1 and T2).

9. In regards to claim 12, Rilly teaches wherein an energy of the inductor current is increased prior to the discharging of the display capacitance or the energy is decreased prior to charging of the display capacitance (fig. 12 IL').

10. In regards to claim 13, Rilly teaches wherein during charging or discharging, the display capacitance is clamped before a stored energy of inductor reaches zero (fig. 9 and 10 Before Ip equals zero Vp is clamped).

11. In regards to claim 14, Rilly teaches wherein the first current path further comprises a diode coupled between the first switch and the first node (D4 (+ and -)).

12. In regards to claim 15, Rilly teaches wherein the second current path further comprises a diode coupled between the first node and the second switch. (D6 (+ and -)).

13. In regards to claim 16, Rilly teaches further comprising: a first clamping circuit coupled between the first and second nodes (D4 (+ and -)); and a second clamping circuit coupled between the first and second nodes . (D6 (+ and -)).

14. In regards to claim 17, Rilly teaches wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path (T4 (+ and -)), and the second clamping circuit comprises a fourth switch (T6 (+ and -))coupled to the first node and a second potential via a second conductive path, wherein the first and second potentials are different (col. 3, lines 10- 46).

15. In regards to claim 18, Rilly teaches wherein the first potential is provide by a positive power source, and the second potential is provided by a negative power source (col. 3, lines 45).

16. In regards to claim 20 Rilly teaches maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path; and maintaining the panel capacitance after step (col.3, lines 10- 45 (fig. 3 T4s circuit) (b) by a second clamping circuit having a fourth

switch coupled to the first node and a second potential via a second conductive path (col. 3, lines 10-45 fig. 3 (T6s circuit).

17. In regards to claim 21, Rilly teaches wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero (col. 4, lines 1-40 and fig. 9 Vp).

18. In regards to claim 22, Rilly teaches wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the inductor current reaching zero (col. 3, lines 10-67 fig. 3 T1 and T2).

19. In regards to claim 23, Rilly teaches wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero (fig. 9 and 10 Before Ip equals zero Vp is clamped).

20. In regards to claim 24, Rilly teaches wherein the second clamping circuit pre-stores energy in the inductor prior to step (a) and the first clamping circuit pre-stores energy in the inductor prior to step (b) (fig. 12 IL' positive and negative).

21. In regards to claim 26, Rilly teaches wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths (fig. 4 T4s and T6s).

22. In regards to claim 27, Rilly teaches wherein the inter-electrode capacitor is charged/discharged based on an LC resonant frequency (col. 3, line 30) of the inductor coil and the inter-electrode capacitor (col. 4, lines 1-8).

23. In regards to claim 28, Rilly teaches wherein the inter-electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor (col. 3, lines 20-67 fig. 3 T1 and T2).

24. In regards to claim 29, Rilly teaches wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero(fig. 9 and 10 Before Ip equals zero Vp is clamped).

25. In regards to claim 30, Rilly teaches wherein the clamping circuit increases an energy of the inductor coil prior to charging/discharging of the inter-electrode capacitor (fig. 12 IL').

26. In regards to claim 31, Rilly teaches wherein each of said first and second switches (fig. 3 (T1 and T2)) comprises a transistor. Examiner notes Rilly teaches using switches but doesn't explicitly teach using transistors as the switches. However, it would have been obvious to one of ordinary skill in the art to use a transistor since TFT are commonly used in plasma displays.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta
January 14, 2008

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER